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EXAMINER	
NADAV,O	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/17/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/965,286	Applicant(s) Gomi et al.
	Examiner ORI NADAV	Group Art Unit 2811

☒ Responsive to communication(s) filed on *Oct 25, 2000* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1, 3, 4, 6, 17, 19, and 20* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1, 3, 4, 6, 17, 19, and 20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *Nov 6, 1997* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a device comprising first, second and third transistors, being formed on one substrate, as recited in claim 17, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1,3, 4, 6, 17, 19 and 20 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. There is no support in the specification for a device comprising first, second and third transistors, being formed on one substrate, as recited in claim 17.

4. There is no support in the specification for a peak position of an impurity concentration of a region formed between the silicon substrate and a base region of the second vertical transistor is deeper than that of a region formed between the silicon substrate and a base region of the first vertical transistor, as recited in claim 1. Although the bottom position of an impurity concentration of a region formed between the silicon substrate and a base region of the second vertical transistor is deeper than that of a region formed between the silicon substrate and a base region of the first vertical transistor, Figure 5 clearly depicts the position of an impurity concentration of a region formed between the silicon substrate and a base region of the second vertical transistor as being equal to that of a region formed between the silicon substrate and a base region of the first vertical transistor.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 3, 4, 6, 17, 19 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. The claimed limitations of a second vertical type transistor whose voltage is different from that of the first vertical type transistor formed on a semiconductor substrate made by forming an epitaxial layer on a silicon substrate, is unclear as to which voltage applicant refers, which element is formed on the semiconductor substrate, which element is made by forming an epitaxial layer, and whether applicant recites two separate substrates or one substrate which is formed of another substrate.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3, 4, 6, 19 and 20, insofar as in compliance with 35 U.S.C. 112, as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. (4,379,726) or Watanabe et al. (4,258,379). Kumamaru et al. teach in figure 10 a semiconductor device comprising a first vertical bipolar transistor 15 and a second vertical type transistor 13 whose voltage is different from that of the first vertical type transistor formed on a semiconductor substrate made by forming an epitaxial layer 11 on a silicon substrate 1, 5, wherein the first transistor

15 has a first embedded diffusion layer 14 formed on an upper part of the substrate and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, the second transistor 13 having a second embedded diffusion layer 5a (figure 8) formed in an upper part of the substrate and having the same conductivity type as the epitaxial layer and having an impurity concentration less than the impurity concentration of the first embedded diffusion layer 14 and is approximately equal to or higher than the impurity concentration of the epitaxial layer (column 3, lines 16 and 27-28) and having a depth greater than a depth of the first embedded diffusion layer, and wherein a peak position of an impurity concentration of a region formed between the silicon substrate and a base region of the second vertical transistor is deeper than that of a region formed between the silicon substrate and a base region of the first vertical transistor.

Watanabe et al. teach in figure 8 a semiconductor device comprising a first vertical bipolar transistor 101 and a second vertical type transistor 201 whose voltage is different from that of the first vertical type transistor formed on a semiconductor substrate made by forming an epitaxial layer 3 on a silicon substrate 1, wherein the first transistor 101 has a first embedded diffusion layer 21 formed on an upper part of the substrate and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, the second transistor 201 having a second embedded

diffusion layer 22" formed in an upper part of the substrate and having the same conductivity type as the epitaxial layer and having an impurity concentration less than the impurity concentration of the first embedded diffusion layer 21 and is approximately equal to or higher than the impurity concentration of the epitaxial layer (figure 9) and having a depth greater than a depth of the first embedded diffusion layer, and wherein a peak position of an impurity concentration of a region formed between the silicon substrate and a base region of the second vertical transistor is deeper than that of a region formed between the silicon substrate and a base region of the first vertical transistor.

Although Kumamaru et al. and Watanabe et al. do not explicitly state a first transistor having a different voltage than that of the second transistor, these features are inherent in Kumamaru et al. and Watanabe et al.s' devices, because Kumamaru et al. and Watanabe et al.s' structures are identical to the claimed structure, and the first and second embedded diffusion layers render the first and second transistors as having two different voltages, respectively. Therefore, the claimed structure is considered to be in at least obvious over prior art's structures.

Regarding claim 3, prior art teach a first embedded diffusion layer having a shallower depth than the second embedded diffusion layer.

Regarding claim 4, prior art teach a second embedded diffusion layer having a impurity concentration at least as high as that of the epitaxial layer.

Regarding claim 6, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15 in Kumamaru et al. and Watanabe et al.s' devices, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 19 and 20, prior art teach a second embedded diffusion layer and an epitaxial layer being an effective collector layers.

10. Claim 17, insofar as in compliance with 35 U.S.C. 112, as in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. or Watanabe et al. in view of Takemoto et al. (4,826,780).
Kumamaru et al. and Watanabe et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a third vertical transistor having a separating diffusion layer formed in the substrate and separating the substrate from a third embedded diffusion layer having an opposite conductivity type to the epitaxial layer.

Takemoto et al. teach in figure 13 a first vertical transistor, a second vertical NPN transistor and a third vertical transistor formed on the substrate, wherein the third vertical transistor having a separating diffusion layer 32 formed in the substrate and separating the substrate 31 from a third embedded diffusion layer 36 having an opposite conductivity type to the epitaxial layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a third vertical transistor on the substrate in Kumamaru et al. and Watanabe et al.'s device, because it is well known in the art to form plurality of transistors of one semiconductor substrate in order to reduce the size of the device. The type of devices which are being formed depend on the requirements of the application in hand.

Response to Arguments

11. Applicant argues on page 2 that there is no support in the specification for a device comprising first, second and third transistors, as recited in claim 17, because figure 5 teaches first and second transistors and figures 11 and 12J teach a third transistor.

Figure 5 depicts one embodiment, whereas figures 11 and 12J depict different embodiments. Applicant can not take elements from one embodiment and combine them with elements of another embodiment, in order to form a new device.

12. Applicant argues on page 3 that Kumamaru et al. do not teach a second embedded diffusion layer having an impurity concentration which is less than that of the first embedded diffusion layer, because layers 12 and 14 have the same impurity concentration, and layer 5a is not an embedded diffusion layer.

The examiner agrees that layers 12 and 14 of Kumamaru et al. have the same impurity concentration. However, the recited second embedded diffusion layer is not layer 12 but layer 5a. Layer 5a is an embedded layer in which impurities are diffused (column 3, lines 28-29), thus rendering it an embedded diffusion layer.

13. Applicant argues on page 4 that Watanabe et al. teach a peak position of an impurity concentration of a region formed between the silicon substrate and a base region of the second vertical transistor being equal to that of a region formed between the silicon substrate and a base region of the first vertical transistor.

Watanabe et al. teach in figure 8 a second embedded diffusion layer 22" being thinner and deeper than the first embedded diffusion layer 21. Therefore, it is clear that the peak position of an impurity concentration of a region formed between the silicon substrate and a base region of the second vertical transistor is deeper than that of a region formed between the silicon substrate and a base region of the first vertical transistor.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

William Mintel

Ori Nadav, Ph.D.

November 9, 2000

William Minte
Primary Exm